Heterogeneous Multi-Die Stitching Enabled by Fine-Pitch and Multi-Height Compressible Microinterconnects (CMIs)

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***Abstract*— A high-density and a highly scalable heterogeneous multi-die integration technology is presented in this paper. Central to this approach is a dense and face-to-face integration of heterogeneous ICs enabled by fine-pitch and multi-height compressible microinterconnects (CMIs) and stitch chips, which serve as the interface through which communication between active ICs occurs. Two separate testbeds are fabricated in order to characterize the proposed integration technology: the first testbed demonstrates the concatenated assembly of chips using the stitch chips with fine-pitch CMIs (in-line pitch of 20 μm), while the second testbed demonstrates the fabrication of multi-height CMIs (75-, 55-, and 30-μm tall CMIs) on the same die. Electrical characterization, including resistance and S-parameters, and mechanical characterization of interconnects are reported as well as the assembly of the testbeds.**

***Index Terms*— 2.5-D/3-D package assembly, compliant interconnects, heterogeneous integration, system in package (SiP).**

I. Introduction

IN THE era of artificial intelligence, cloud computing, Internet of things, big data, and autonomous computing, there is a significant need for the seamless integration of heterogeneous multi-die in a small footprint with high-performance interconnects [1]–[4]. This need has been fulfilled until recently by integrating analog, digital, and limited sensor/MEMS functionalities into a monolithic system-on-chip (SoC) architecture. However, the surging development cost and time associated with monolithic SoC designs combined with the limited materials and heterogeneous devices that can be incorporated make monolithic processes more challenging going forward. This has promoted significant research in several heterogeneous multi-die integration technologies by virtue of their integration flexibility and faster time to market, which has led to solutions including silicon interposer [5]–[7], embedded multi-chip interconnect bridge (EMIB) technology [8], [9], and silicon-less interconnect technology (SLIT) [10]. However, while these approaches have clear advantages, they also have a number of challenges that may limit their utilization in multi-die microsystems. For example, silicon interposers require through-silicon vias (TSVs), which add cost, fabrication complexity, and are, in general, limited by reticle size. Table I summarizes and compares key features of each of these heterogeneous multi-die integration technologies.

In this paper, we propose a TSV-less heterogeneous integration technology, as illustrated in Fig. 1. Our approach seeks to form concatenated ICs using heterogeneous IP blocks (from multiple foundries) enabled by a combination of 2.5-D integration and face-to-face 3-D integration technologies. To this end, we utilize a combination of solder bumps and mechanically elastic, multi-height, and fine-pitch compressible microinterconnects (CMIs) to robustly assemble the ICs. As shown in Fig. 1, the fine-pitch (as small as 20 μm) CMIs are used to provide the dense signaling pathways between the concatenated "anchor ICs" through the stitch chips. Multi-height CMIs are used to provide face-to-face interconnections between the anchor ICs and the "surface-embedded ICs" irrespective of any possible IC thickness differences; this enables high-density face-to-face interconnection of dice while maintaining low system footprint. Solder bumps with larger pitch and height are used for power delivery, signal routing between the die and the package, and mechanical interconnection between the anchor ICs and the package. The solder bumps also create the necessary force for the CMIs to form pressure-based reliable contacts. The stitch chips that may contain high-quality passives and/or active circuits, in the simplest form contain only dense interconnects to interconnect nearby active anchor ICs. The anchor IC may be a logic, field-programmable gate array (FPGA), monolithic microwave integrated circuit (MMIC), or photonic die, etc., and the

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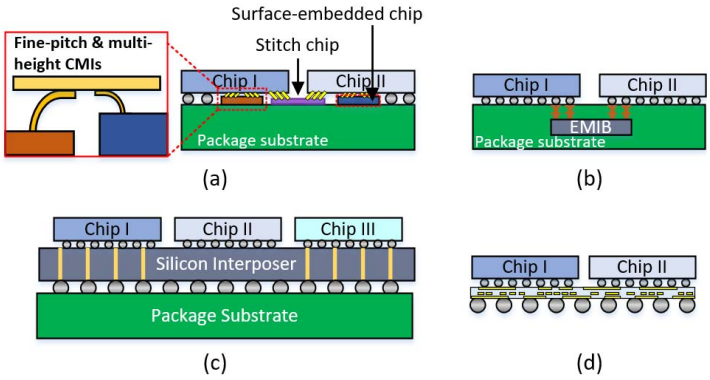
TABLE I
COMPARISON OF HETEROGENEOUS MULTI-DIE INTEGRATION SOLUTIONS

	(a) This work	(b) EMIB [8], [9]	(c) Silicon Interposer [5]-[7]	(d) SLIT [10]
Integration architecture				
Interconnect type	**Compressible interconnect** + Bumps	Bumps	Bumps + **TSV**	Bumps
Ability to compensate for surface/thickness variation	**High**	Limited	Limited	Limited
I/O pitch	**20 µm**	55 µm	30-60 µm	45 µm
System scalability	Scalable	Scalable	Limited	Limited
Agnostic to package substrate	**Yes**	No	-	-

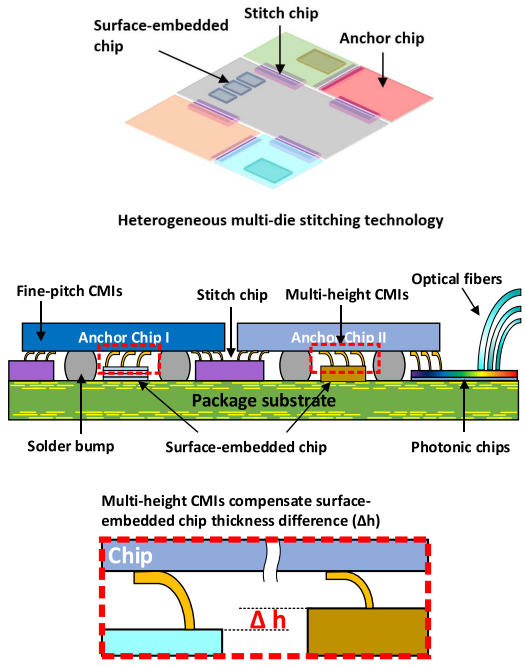


Fig. 1. Schematic of heterogeneous multi-die stitching technology enabled by fine-pitch and multi-height CMIs.

surface-embedded IC may be a dense decoupling capacitor die, memory die (or stack), MEMS die, or an integrated passive device die, for example. In Fig. 1, we illustrate an approach where a silicon photonic integrated circuit with direct access to fiber assembly is face-to-face interconnected to an anchor IC (i.e., logic or FPGA) using the CMIs.

The advantages of CMIs in this multi-die heterogeneous integration approach are their ability to mechanically compensate for surface nonplanarity of a substrate, stitch chip thickness variations, and interconnection gap differences between the anchor and surface-embedded ICs as a single anchor IC may be interfaced to multiple stitch chips on all four edges and to multiple surface-embedded ICs of different thicknesses. To be specific, the benefits of CMIs over conventional solder bump interconnects for multi-die heterogeneous integration are the following: 1) CMIs are not susceptible to bump bridging [11], [12], which is a more prevalent issue as pitch is scaled down, since they are pressure-based interconnects and do not reflow during the assembly process; 2) owing to their mechanical flexibility, CMIs can reduce the restrictions on stitch chip and surface-embedded IC thickness variations and overcome surface nonplanarity of an organic substrate, thus improving assembly yield and providing for unique integration options; 3) CMIs eliminate the need for strict uniformity control on microbump height; and 4) CMIs enable multi-height face-to-face 3-D bonding that is challenging by using conventional microbump solutions. Since the proposed approach is not reticle size limited as it is for silicon interposers and SLIT, it allows one to build highly scalable and dense electronic systems.

This paper is organized as follows. Section II describes the fabrication and assembly process of the proposed integration approach. The fabrication of multi-height CMIs is also described in Section II. In Section III, the mechanical and electrical characteristics are measured, and Section IV concludes this paper.

II. FABRICATION AND ASSEMBLY

The overall integration process flow used in this paper is shown in Fig. 2. The integration process begins with fabricating solder bumps on the package substrate. Next, the stitch chips and/or surface-embedded ICs are assembled onto the

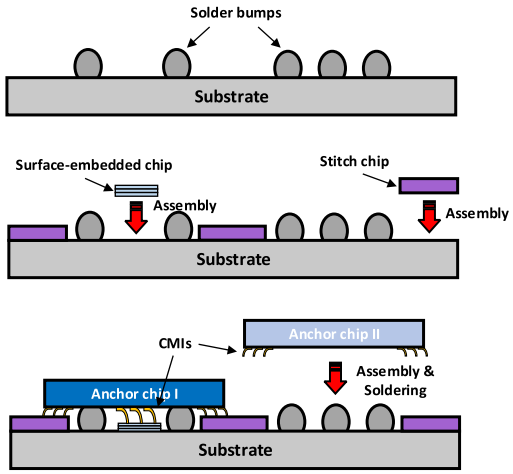


Fig. 2. Integration process flow.

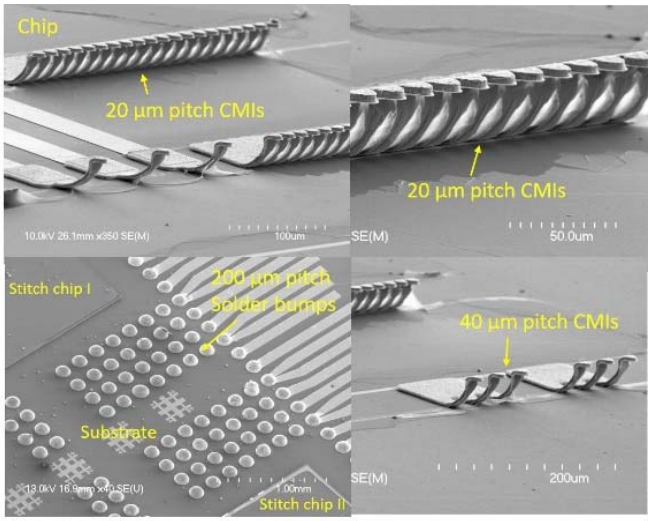


Fig. 3. SEM images of the solder bumps and fine-pitch (20 μm in-line pitch) CMIs on the substrate and chip, respectively.

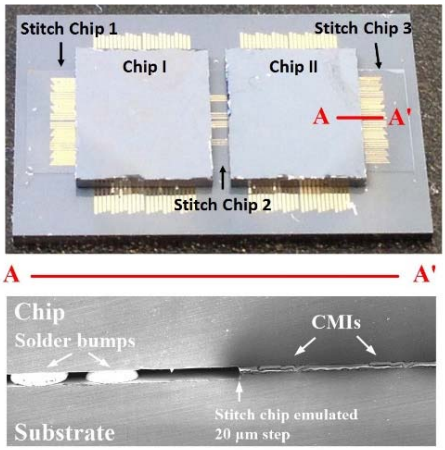


Fig. 4. Optical and SEM cross-sectional images of the assembled testbed.

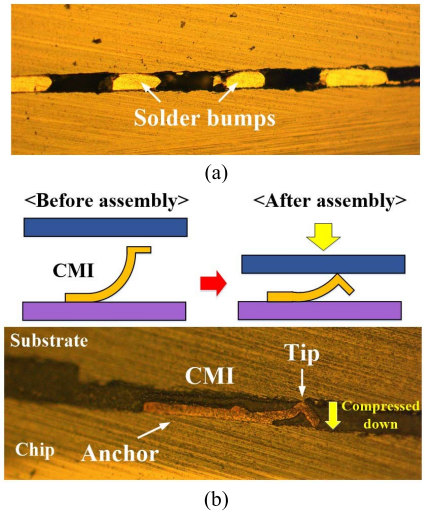


Fig. 5. Optical microscope cross-sectional image of (a) solder bumps and (b) CMI.

package substrate. Finally, the anchor dice with fine-pitch and multi-height electroless gold plated NiW CMIs are flip-chip bonded onto the package substrate, as shown in Fig. 2. NiW is used for the fabrication of the CMIs due to its high yield strength (1.93 GPa); for reference, electroplated Cu, under specific plating conditions, has a reported yield strength of 136 MPa [13]. This high yield strength enables the CMI to tolerate more stress before experiencing plastic deformation during compression. The detailed fabrication process of CMIs is described in [14]. In this paper, we extend this prior work by introducing multi-height CMIs, for the first time, and demonstrate the assembly results of the system as shown in Fig. 1. To this end, two separate experimental testbeds are pursued in order to demonstrate the key features of the proposed heterogeneous integration technology: 1) assembly of chips with fine-pitch CMIs on a substrate containing stitch chips of different thicknesses and solder bumps and 2) assembly of a chip with multi-height (three different heights) CMIs onto a substrate with gold pads.

In the first testbed, a stitch chip on the package is emulated using a 20-μm tall step (though a larger step is possible) and the fine-pitch CMIs are fabricated on the assembled dice. The fabricated solder bumps are approximately 50 μm in height (in general, solder bumps with larger pitch can be made taller than 100 μm [15]) and 200 μm in pitch while the lithographically defined CMIs are approximately 40 μm in height and formed on a 20-μm in-line pitch, as shown in Fig. 3. The fine-pitch CMIs provide high I/O density for signaling between the anchor dice connected through the stitch chips. An approximately tapered CMI design is adopted in order to distribute the stress along the body during deflection; this increases the vertical elastic range of motion. The upward-curved CMI design ensures that the tip of the CMI remains in contact with the receiving pad during deflection (i.e., assembly).

Optical and SEM cross-sectional images of the assembled testbed are shown in Figs. 4 and 5. The dice are assembled by a thermocompression bonding process using a Finetech Fineplacer Lambda flip-chip bonder. Once the dice are aligned to the substrate, thermocompression bonding compresses CMIs downward while reflowing the solder bumps. Next, the reflowed solder bumps are solidified; this provides the necessary mechanical interconnection between

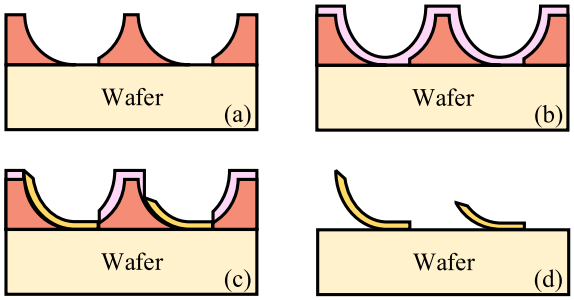


Fig. 6. Schematic fabrication process of the multi-height CMIs. (a) Photoresist patterning. (b) Seed layer sputtering followed by photoresist coating. (c) CMI mold patterning and electroplating. (d) Releasing.

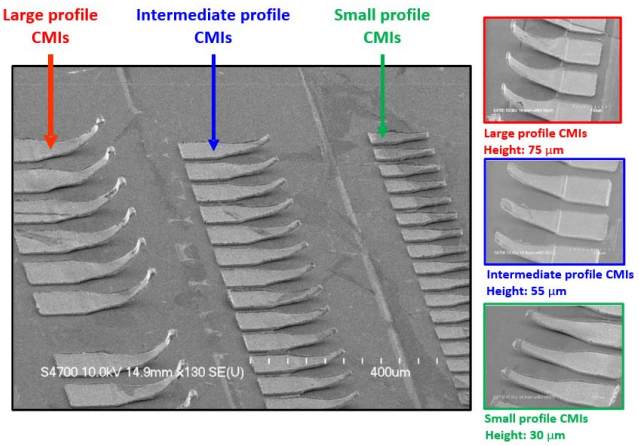


Fig. 7. SEM images of the fabricated multi-height CMIs (75, 55, and 30 μm).

the substrate and anchor ICs, which maintains the CMIs in a compressed state after assembly, ensuring reliable interconnections. The two anchor dice in Fig. 4 are placed side by side onto the three stitch regions and the substrate. As shown in Fig. 5, the center of the dice is bonded to the substrate using solder bumps, while two edges of the die are suspended above the silicon steps (i.e., the "stitch chips") and supported by the fine-pitch CMIs. As shown in Fig. 5(b), the CMIs are compressed downward during assembly and form a pressure-based contact with the substrate.

Next, chips containing three different CMI heights are batch fabricated for the second testbed. Fig. 6 illustrates the fabrication process of the multi-height CMIs. The process begins with spin coating of a sacrificial photoresist layer followed by photolithographic patterning to yield a curved sidewall profile [14]. Next, a Ti/Cu/Ti seed layer and a second photoresist layer are deposited for electroplating. During the lithography process of the second photoresist layer, CMIs with multiple heights can be easily patterned by exposing different areas on the curved sidewall profile, as shown in Fig. 6(c). After patterning the molds with various heights, NiW is electroplated within the molds to form the multi-height CMIs. Next, the photoresist layers and Ti/Cu/Ti seed layer are removed, leaving behind freestanding multi-height CMIs. Finally, CMIs are passivated by electroless gold plating to prevent the oxidation of NiW and to decrease the resistance of the CMIs [16]. Fig. 7 shows the SEM images of the fabricated multi-height CMIs. The heights of the fabricated CMIs are 75, 55, and 30 μm, and their in-line pitch is 150 μm. In order to integrate surface-embedded ICs of various thicknesses between the package substrate and the anchor ICs, as shown in Fig. 1, the height of the CMIs can be easily adjusted accordingly during fabrication.

III. Mechanical and Electrical Characterization

Mechanical compliance, a key property of CMIs, is measured using a Hysistron Triboindenter with a conospherical probe tip, as illustrated in Fig. 8. The conospherical probe tip was directly positioned on the flat top area of the CMI; in each indentation cycle, the probe tip moves downward to a preset depth and then upward while measuring the reaction force from the CMIs. First, three 40-μm tall fine-pitch CMIs fabricated on different regions of the chip were indented and

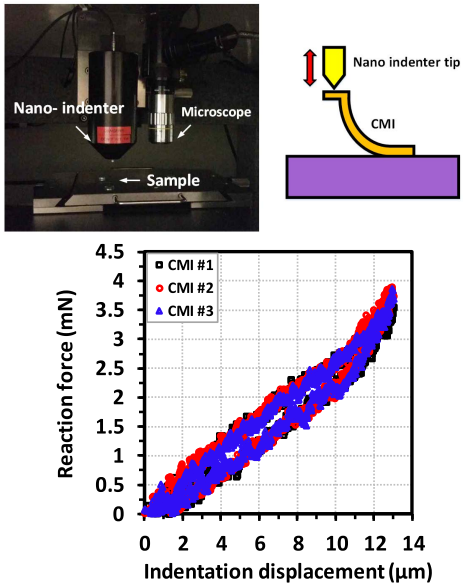


Fig. 8. Compliance measurement setup and reaction force versus indentation displacement graph of the 40-μm tall CMIs.

the results of the indentation tests are shown in Fig. 8. The average compliance of the CMIs is approximately 3.47 mm/N, and the similar value of compliance was obtained for the tested CMIs.

As shown in Fig. 8, the 40-μm tall CMIs designed under consideration achieve up to 13 μm of vertical elastic range of motion. Even if CMIs experience plastic deformation after being compressed by more than 13 μm, mechanical failure does not occur, and hence, they can still compensate for a large stitch chip thickness variation (equal to the original height of the CMIs). Therefore, CMIs can maintain the pressure-based contact between the stitch chip and dice after assembly, as shown in Fig. 5(b). However, the mechanical attributes of the CMIs can be widely engineered due to the large design window afforded by the fabrication process; CMI properties can vary greatly depending on their lithographically defined mold design, their thickness, their electroplated material, their height, and so on [14]. To test the lifetime fatigue reliability of the CMIs, one of the 75-μm tall CMIs (from the multi-height CMIs wafer) was consecutively indented by 30 μm for

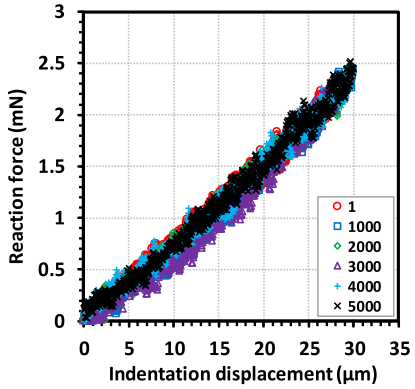


Fig. 9. 5000 indentation cycles graph of the 75-μm tall CMI.

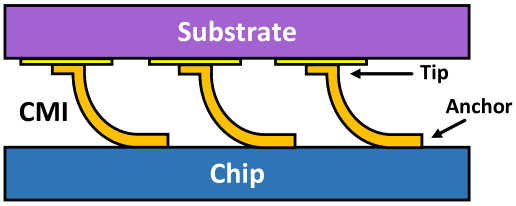


Fig. 10. Cross-sectional schematic of the flip-chip bonded sample with 75-μm tall CMIs.

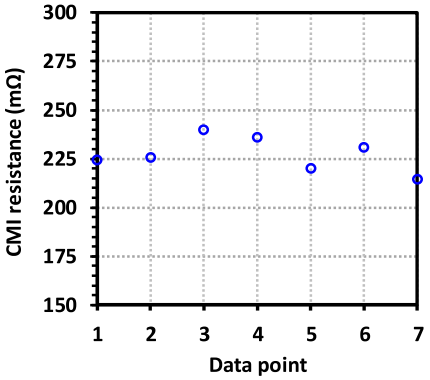


Fig. 11. Four-point resistance of the 75-μm tall CMIs including contact resistance with gold traces.

5000 cycles. The CMI consistently returned to its original position during the 5000 indentation cycles, as shown in Fig. 9.

The four-point resistances of the interconnections after assembly were measured using a Karl–Suss probe station. First, a chip containing multi-height CMIs was bonded to a Si substrate containing gold traces, as shown in Fig. 10. In this testbed, the 75-μm tall CMIs were measured as a representative structure. The chip and the substrate were held in place with epoxy to facilitate the measurements. The average postassembly resistance of the 75-μm tall CMIs in contact with the Au traces is 227.2 mΩ, as shown in Fig. 11.

Next, chips containing fine-pitch CMIs were flip-chip bonded onto three substrates containing different stitch chip thickness mismatches (Δt = 0, 10, and 20 μm) and the solder bumps, as shown in Fig. 12, in order to demonstrate multi-height face-to-face interconnection. The resistances of the CMIs in contact with the gold traces on the multi-height stitch chips were measured. The solder bumps were reflowed after assembly and their four-point resistance measurements

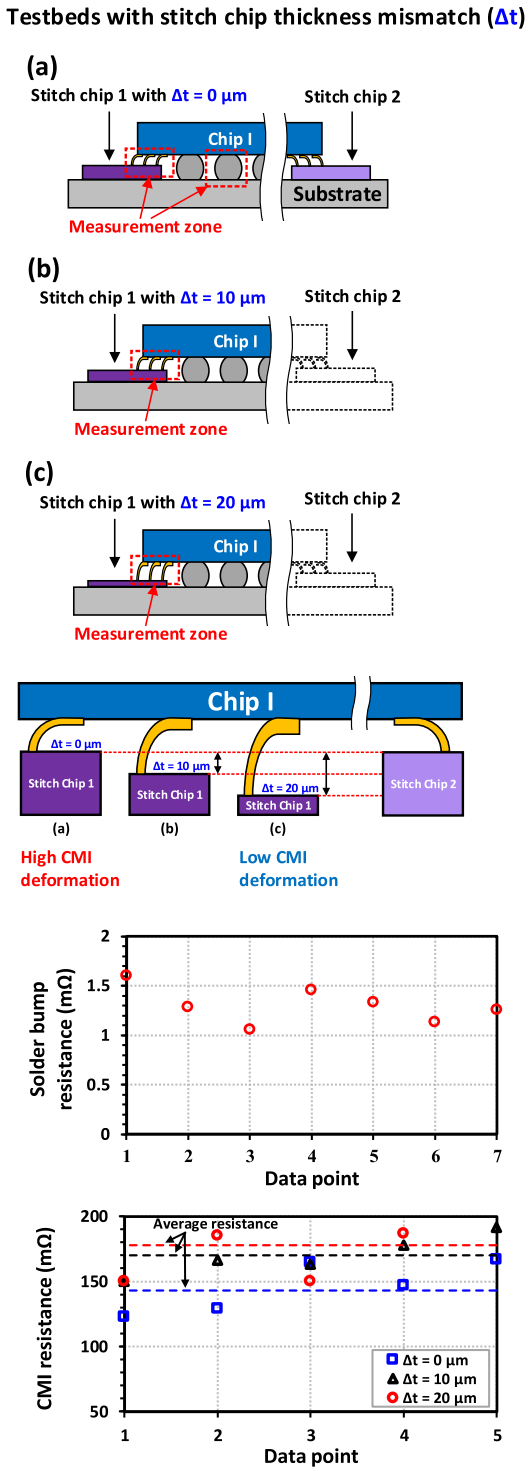


Fig. 12. Four-point resistance measurement results of the solder bumps and fine-pitch CMIs. Stitch chip thickness mismatch of the testbeds at (a) 0 μm, (b) 10 μm, and (c) 20 μm, respectively.

were also measured. Note that no epoxy was used in this testbed since solder bumps were used for the mechanical interconnection. As shown in Fig. 12, the average resistance of the CMIs, including their contact resistance with the gold traces on the substrate, is 146.31, 170.02, and 176.71 mΩ, respectively, for Δt = 0 (i.e., thicker stitch chip), 10, and 20 μm (i.e., thinner stitch chip) thickness mismatch. We suspect that the contact resistance between the CMIs and the pads contributes

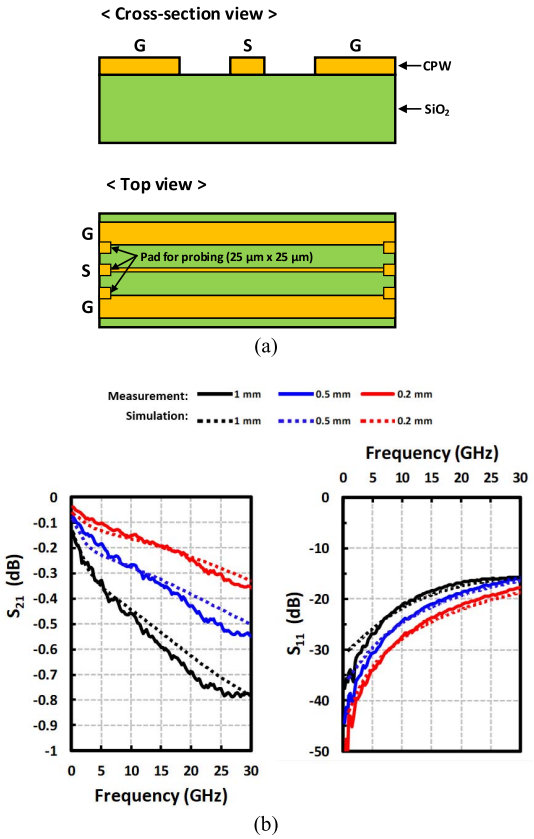


Fig. 13. Schematics of (a) CPW and (b) measured S_{21} and S_{11} of the CPW for three wire lengths.

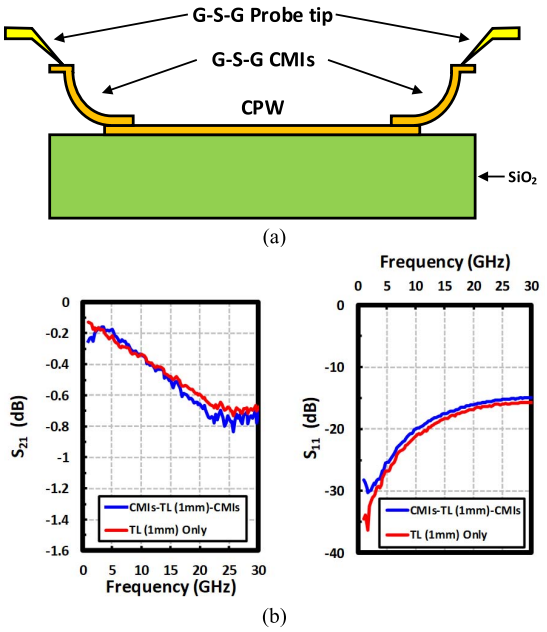


Fig. 14. Schematic of the cross section view of the (a) measured CMIs-TL (1 mm)-CMIs structure and (b) measured S_{21} and S_{11} results.

to the difference in the average resistances seen in Fig. 12 since a thicker stitch chip deforms the CMI more than a thinner stitch chip; this affects the contact force, and hence, the contact resistance of the CMIs. The average resistance of the solder bumps is 1.31 mΩ and we again suspect that variations from the fabrication process contributed to the resistance variation. These four-point resistance measurement results confirm that the CMIs can maintain electrical connections between the die and the stitch chips even when there is a stitch chip thickness mismatch resulting perhaps from using dice from different foundries. As noted earlier, even though up to 20 μm of stitch chip thickness mismatch has been fabricated in this demonstration, CMIs can compensate for any stitch chip thickness variation or surface nonplanarity of the substrate up to their original height owing to their mechanical flexibility.

In order to gain initial insight into the frequency response of the CMIs, transmission lines (TLs) with and without the CMIs were fabricated and measured. First, coplanar waveguides (CPW) of various lengths were fabricated on a silicon substrate, which contained a metal layer near the silicon, as shown in Fig. 13(a). A SiO_2 dielectric layer with 5 μm of thickness was used under the CPW. The Cu TL with Au coating is 9 μm wide and 2 μm in thickness. The Au layer is 50 nm thick and was deposited on top of the Cu layer to prevent oxidation. The dimensions of the TL were calculated to yield characteristic impedance (Z_0) of 50 Ω using high frequency structure simulator (HFSS). Pads with dimension of 25 × 25 μm^2 are added to both ends of the TL for probing. The fabricated TLs were measured using an Agilent N5245A network analyzer up to 30 GHz. The measured S_{21} and S_{11} for TL lengths of 0.2, 0.5, and 1 mm are shown in Fig. 13(b). HFSS simulation results are compared with the measured results and show a good agreement. A clear tradeoff between the loss and TL length can be observed as expected: this is important as it imposes a limit on the distance between adjacent anchor ICs. Next, CMIs were fabricated on each end of the 1-mm long TLs, and S-parameters of the stitch chip channels through CMIs-TL-CMIs were measured by directly probing the flat tip of the CMIs, as shown in Fig. 14(a). Fig. 14(b) shows the measured S_{21} and S_{11} results; the maximum insertion loss is approximately 0.8 dB while the reflection loss is less than 10 dB. As shown in Fig. 14, CMIs add minor loss compared to the loss of a standalone TL; thus, if the length of TL is less than 1 mm (i.e., 0.2-mm or 0.5-mm TL, as shown in Fig. 13), the insertion loss of interconnections through the stitch chip can be comparable to the insertion loss of TSVs from the literature [17]–[19]. Therefore, based on the initial high-frequency measurement, the proposed integration approach has the potential for low-loss signal interconnections at high-frequency.

IV. Conclusion

This paper presents the fabrication and assembly process of a heterogeneous multi-die integration approach enabled by fine-pitch and multi-height CMIs. Mechanical and electrical characterizations of the assembled fine-pitch and multi-height CMIs were performed, and measured results are presented to demonstrate early success. Four-point resistance measurement results for both solder bumps and fine-pitch CMIs show robust signal interconnect routing between two anchor dice through stitch chips with low resistance variation. RF performance measurement results also show that the measured CMIs add negligible performance degradation on the stitch chip

channels. Indentation measurement results demonstrate the compliance of CMIs and its flexibility on mechanical deformation. These results demonstrate a superior mechanical advantage when compared to conventional microbumps. SEM images of the fabricated multi-height CMIs show repeatable structures of different height profiles. The approach is proposed to achieve dense signaling between ICs in addition to providing a highly scalable and versatile heterogeneous IC integration solution and a face-to-face 3-D IC bonding interface that extends beyond the reticle limits of traditional multi-die integration solutions.

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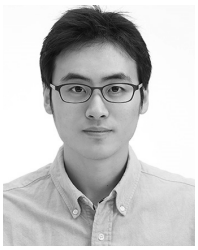

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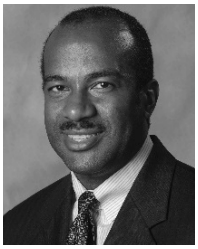

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